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Fabrication of Semiconductor Nanowires for Electronic Transport Measurements

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Abstract: We report on epitaxial growth of InAs nanowires and the steps necessary to create devices for electronic transport experiments. Growth conditions were found by the use of metal organic vapor phase epitaxy (MOVPE) resulting in nanowires with designable length and diameter. Electrical properties indicate diffusive electron transport with an elastic mean free path of around hundred nanometers. Coherent quantum mechanical effects and single electron tunneling can be observed at low temperatures in quantum dots created along the nanowire. We demonstrate the realization of highly tunable quantum dots with metallic top-gates. Beyond that, alternative techniques to introduce potential barriers based on local constrictions are investigated.

Keywords: Advanced materials · Indium arsenide compounds · Nanowires · Quantum dots · Semiconductors

1. Introduction

State of the art semiconductor technology follows the route of further miniaturization of structures defined by lithographic methods on planar substrates. As an alternative way, the use of as-grown nano-objects to assemble electronic devices 'bottom-up' has been discussed [1]. In these devices, quantum mechanics can have a significant influence on the physical properties and may even lead to new functionality.

Nanometer-size structures weakly coupled to electric contacts, so called quantum dots, are generally considered as the fundamental functional unit in nanoelectronic devices. As demonstrated in various experiments, single charges and spins can be controlled with high precision in quantum dots [2][3]. Many proposals therefore suggest quantum dots as a possible realization of quantum bits (qubits) in solid-state based quantum computers and quantum information processing schemes [4].

Special interest is paid to the spin degree of freedom. An important motivation is that coherence times can be much larger for spin than for charge in solid-state systems [5][6], since spins are only weakly coupled to electric fluctuations of the environment.

This leads to the vision of 'spintronics' instead of pure electronics. InAs is an appropriate semiconductor material for building spintronic devices because of its strong spin-orbit interaction and the large effective g-factor. In addition, the very small effective electron mass leads to strong quantum confinement effects and hence to large energy level spacings, making it experimentally feasible to observe quantum mechanical effects.

Nanowires grown from InAs combine the properties mentioned above: narrow confinement in lateral directions without the need for lithographic steps and promising spin-related properties. They appear to be an interesting alternative to the extensively studied carbon nanotubes (CNT), where the difficulty to control whether the tube is semiconducting or metallic before contacting makes specific device fabrication rather challenging.

2. Growth of InAs Nanowires

Our goal is to fabricate single-crystalline InAs nanowires of several micrometers length in order to make processing for electrical contacts feasible. To observe quantum effects at temperatures accessible with standard low temperature equipment (T = 30 mK up to 4.2 K), the wires should have a width of less than 200 nm.

2.1. *Catalytic Nanowire Growth*

Growth of semiconductor nanowires has been accomplished with several different growth techniques. A very controllable approach is the catalytic growth from metallic nanoparticles which are distributed on the growth substrate (Fig. 1). This was first

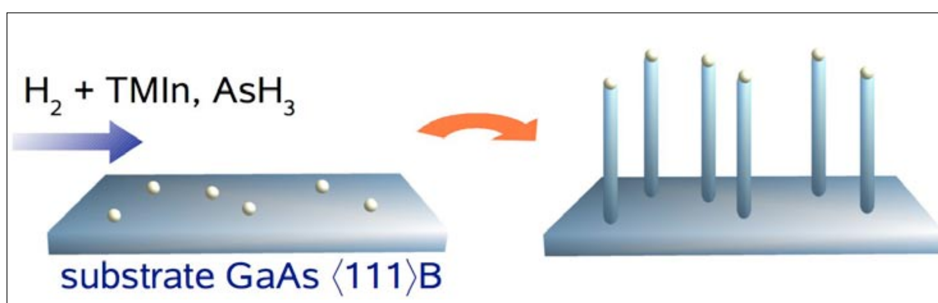

Fig. 1. The principle of nanowire growth from catalytic Au nanoparticles (yellow spheres)

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explained and demonstrated for Si nanowhiskers by Wagner and Ellis [7] and was extensively studied for III-V-semiconductors (see [8] and references therein).

It is widely accepted that the catalytic growth process is based on the vapor-liquid-solid (VLS) mechanism. Here, the growth is fed by precursors in the gas phase surrounding the catalytic nanoparticle and the substrate. The growth species and the metal catalysts form a eutectic alloy at a temperature below the melting point of the semiconductor. The metal catalyst itself should be insoluble in the materials to be grown. For most III-V-semiconductors this condition is met by Au, but also growth from Pt, Pd, Ni, Fe has been demonstrated. The driving force of the growth is a supersaturation of source materials in the alloy, which can ideally only be reduced by nucleation at the liquid–solid interface. This way only longitudinal growth takes place, as long as the temperature does not rise above a critical value where usual bulk growth in lateral direction becomes thermodynamically favorable. A choice of properly sized Au particles allows straight-forward control of the average diameter of the nanowires. The position of the nanowire to be grown is also well defined by the catalytic particle. This high degree of control is crucial for an up-scaling of the growth process which would be necessary for eventual nanowire applications.

2.2. *Growth with Metal Organic Vapor Phase Epitaxy*

Several different epitaxy schemes have been successfully applied to grow nanowires [8], such as Metal-Organic Vapor Phase Epitaxy (MOVPE), Chemical Beam Epitaxy (CBE), Molecular Beam Epitaxy (MBE) and laser ablation.

We use MOVPE [9][10] starting from almost mono-disperse, colloidal Au nanoparticles which are randomly distributed on the growth substrate. For InAs nanowires growth, trimethyl-indium (TMI) and arsine (AsH_3) were used as precursors in a constant carrier flow of hydrogen (H_2). In contrast to CBE and MBE, which are ultra-high vacuum approaches where the precursors are brought to the substrate in a focused beam, a gas phase with a total pressure of around 100 mbar surrounds the substrate. This leads to higher growth rates of typically 10 nm/s in longitudinal direction compared to about one atomic monolayer per second in CBE [11]. An obvious disadvantage of this is stronger gas diffusion making it more difficult to grow heterostructures with sharp interfaces, since this requires instantaneous changes of the source materials at the growth interface [10][12][13].

The surface of the growth substrates should be free of native oxide. We used commercial Epi-ready wafers. Colloidal Au particles with different diameters (20 nm, 40 nm, 60 nm, 100 nm) were dispersed on the substrate.

Crucial parameters influencing the nanowire growth are the growth temperature, the crystallographic orientation of the substrate surface and the partial pressures of the group-III and group-V precursors. We focus on the growth of InAs nanowires on GaAs <111>B and InP <001> surfaces. The process is performed under low-pressure MOVPE conditions with 100 mbar total pressure. In our study, we fixed the partial pressures for AsH_3 (8.2×10^{-2} mbar) and TMIn (1.5×10^{-3} mbar). Fig. 2 shows the results of InAs nanowires grown for 15 minutes on GaAs <111>B surfaces.

All three growth runs were catalyzed by Au particles with 40 nm diameter. The length distribution of the wires depends strongly on the reactor temperature. For the lower temperatures, we find wires as long as 30 μm but with strong variations in the length. At T = 465 °C, the length distribution is quite narrow around 7 μm.

From Fig. 2 it is striking that, especially for higher temperatures, the nanowires are tapered from base to top. Typical widths are up to 150 nm at the bottom and less than a few tens nanometer at the tip.

These observations, together with an obviously reduced growth rate at the higher temperature (Fig. 2) are expected from kinetically activated competition between radial shell growth and the axial VLS growth for temperatures rising above the eutectic regime. The above findings are in agreement with detailed studies of the growth kinetics for different III-V-semiconductor nanowhiskers [10].

There are many experimental observations by different groups using various epitaxy methods that are not understood in detail. For example, InAs nanowire growth has been demonstrated at temperatures clearly below the eutectic point of Au/In, which casts doubt on the validity of the VLS mechanism [14]. This and other ambiguities are attributed to a significant change of the phase diagram and the details about the eutectic regime for structures on the nanometer scale. For our purpose, however, growth with the conditions described above leads to a sufficient portion of nanowires which are long and homogenous enough for electrical contacting as described in Section 3.1.

2.3. *Stacking Faults*

It was already pointed out by Hiruma *et. al.* [9], that for growth on GaAs <111>B surfaces, the InAs nanowires are not single-crystalline in a strict sense. Under the described conditions, InAs whiskers show perfect hexagonal cross sections, as can be clearly seen in Fig. 2d. The two maximally close-packings leading to this structure are the zinc-blende and the wurzite lattice. Be-

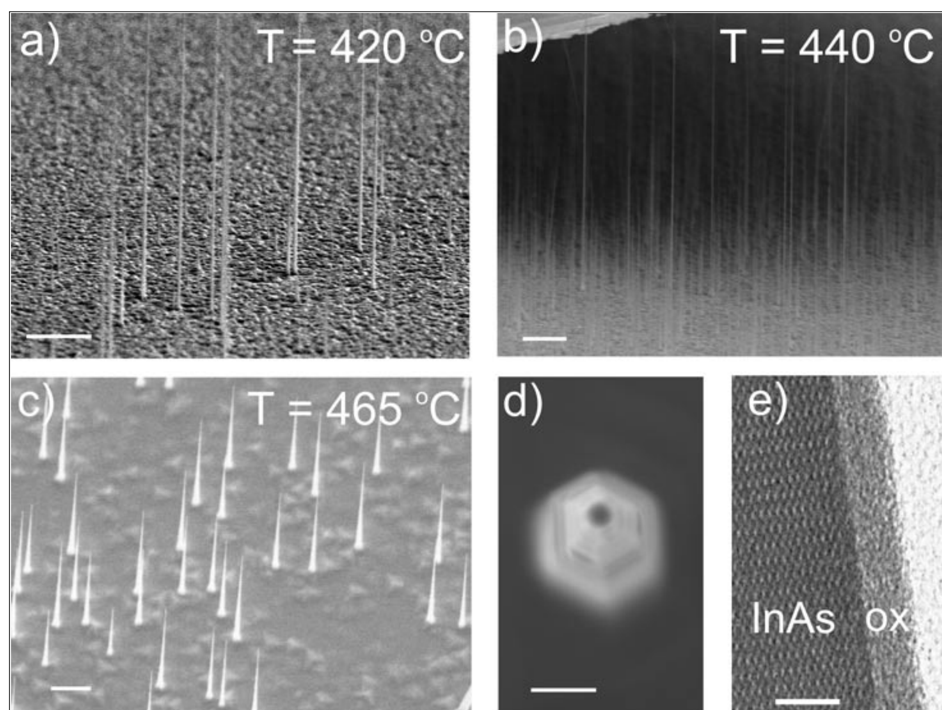

Fig. 2. a)–c) Scanning electron microscope (SEM) images of InAs nanowires grown on GaAs <111>B surface from 40 nm Au particles for three different growth temperatures. Growth time was 15 min. The longitudinal growth rate is smallest for T = 465 °C. For a) and b) tilted view 80°, scale bar 1 μm; c) tilted view 30° scale bar 2 μm. d) Top view SEM image showing the hexagonal cross section for growth in <111> orientation; scale bar 100 nm. e) Transmission electron microscope (TEM) image showing the crystal lattice and the surface oxide (ox.) of a wire from b); scale bar 3nm.

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cause of the energetic equivalence, there is the possibility for stacking faults between (111) layers of the zinc-blende lattices and their rotational twins. These planes are turned by 180° around the [111] growth direction and a pair of a plane and its rotational twin constitute a single (001) wurzite plane at the boundary. This way, segments of zinc-blende and wurzite can be generated along the nanowire by twining planes.

Although the preferred crystal structure can be determined to some extent by the other growth conditions [9] (especially temperature and ratio of the group III and V precursors), the described stacking faults are frequently observed for growth on GaAs (111)B surfaces. Their typical separation ranges from a few nanometers up to several hundred nanometers. It has been argued that this reduces the electronic mean free path to values shorter than expected for epitaxially grown crystalline structures.

Different from (111) substrates, nanowires emerge with square cross section for growth in <001> direction. In this case, stacking faults are very rare due to the lack of energetically equivalent twinning planes. Perfect defect-free structures have been found on (001) oriented substrates for InP nanowires [10]. As an approach to overcome the problem of electron scattering at stacking faults, we investigated InAs nanowires grown on (001) InP substrates. As can be seen in Fig. 3, most of the nanowires still grow along the two equivalent <–1–1–1> directions. Nevertheless there are some whiskers growing perpendicular to the (001) surface, which clearly have a square cross section. We find that the growth rate for the [001] orientation is much smaller than for <–1–1–1>. Compared to typically 10 µm for <–1–1–1>, the <001> wires only reach lengths of about 3 µm after 15 min of growth.

3. Electrical Transport Measurements

3.1. *Contacts to Individual Nanowires*

From the technological point of view, a major advantage of the InAs semiconductor is its tendency to form highly transparent electrical contacts to many metals [15][16]. A narrow band gap of 350 meV (compared to 1.4 eV in GaAs) avoids the formation of high Schottky barriers. For the bulk material it is furthermore known that the Fermi level is pinned in the conduction band at the surface [17][18] which avoids the formation of a Schottky contact if a metal is deposited. This is in sharp contrast to other commonly used semiconductors like silicon or GaAs. In those materials, electronic surface depletion requires intricate alloying procedures to obtain ohmic contacts of the electron gas in the semiconductor to metals.

After growth, the nanowires are transferred to a conductive, degenerately n-doped Si substrate with a 300 nm insulating SiO_2 over-layer. A conventional method for this transfer is to dissolve the nanowires in a small amount of ethanol using ultrasonic pulses to break the wires off the substrate and subsequently putting a microliter droplet of the solution on the silicon chip. We also achieved good results by simply mechanically brushing the nanowires from the growth sample and tipping onto the Si substrate with a piece of clean paper. For thin nanowires with diameters smaller than 100 nm, it is crucial that the Si substrate contains markers with specified positions. The nanowires are then located with a scanning electron microscope (SEM) and contact electrodes can be fabricated relative to the markers using electron beam lithography (EBL). Fig. 4a shows an SEM image of a sample, where a long InAs nanowire with <111> growth direction and a short <001> wire with square cross section are contacted simultaneously.

Thicker wires with diameters larger than 100 nm are clearly visible in an optical microscope with magnification of 200. For these nanowires we use a much simpler procedure based on a single step optical lithography. After transfer on a Si/SiO_2 chip without the need for predefined markers, the nanowires are optically located in a standard mask aligner and contacts are defined with an optical mask containing four electrode fingers with a fixed separation of 1.5 micrometers. An example is shown in Fig. 4b.

In order to achieve good ohmic contacts, the native semiconductor oxide (see Fig. 2e)) must be removed from the contact surfaces before metallization. Good results are achieved with the commonly used etch treatment in a buffered HF solution [19]. One disadvantage of this etchant is that it also reacts with the insulating SiO_2 layer leading to current leakage in later electronic measurements. Another issue is the rapid reoxidation of the surface [20]. We found much more reliable contacting with about 90% yield using a simultaneous etching and surface passivation scheme: A highly diluted (1:1000) ammonium-polysulfate ($(NH_4)_2S_X$) solution removes oxide efficiently and provides protection against reoxidation during the transfer of the samples to the metal evaporation equipment [21][22]. The InAs nanowires themselves and the SiO_2 substrate are almost unaffected by this procedure. After the lithographic steps and etching, a titanium 'wetting' layer of 20 nm thickness followed by about 180 nm Au are deposited as electrode material.

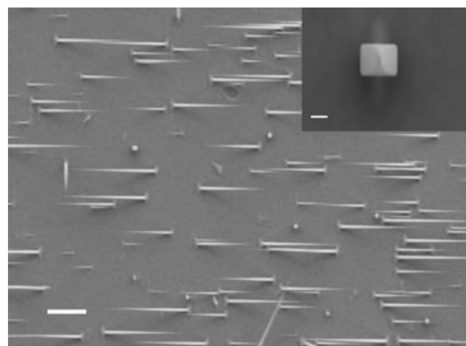

Fig. 3. Top view SEM image of InAs nanowires grown on (001) InP substrate at T = 440 °C from 40 nm Au particle for 15 min. Most of the wires grow in <–1–1–1> directions (left and right). Wires growing perpendicular to the surface in [001] orientation have a quadratic cross section (inset). Growth rates for <001> are much smaller than for <–1–1–1> orientation. Scale bars are 2 µm (main figure) and 100 nm (inset).

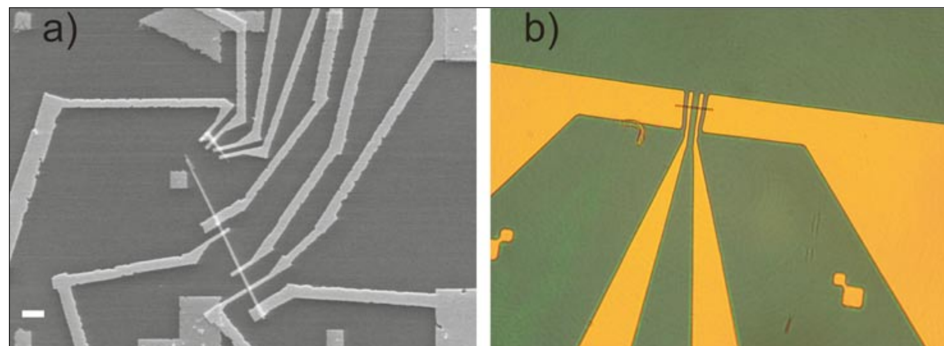

Fig. 4. a) SEM image of a long <111> InAs nanowire and a short <001> nanowire contacted by EBL on a Si/SiO_2 substrate (see text). Alignment markers are also visible. b) Optical microscope image of a thicker nanowire contacted with optical lithography. The separation between the contact fingers is 1.5 µm.

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3.2. *Electrical Characterization*

The accumulation of charge carriers at the surface of bulk InAs does not straightforwardly imply the same behavior for nanometer-sized wires. Nevertheless, other groups have already reported on ohmic contacts to InAs nanowires with excellent quality, even better than to interfaces between metal and bulk InAs [16][23]. We measured two-terminal resistances of several kΩ/μm wire length at room temperature for <111> InAs wires as shown in Fig. 5. From four-terminal measurements on devices like those in Fig. 4, where a current is driven between the outer pair of electrodes and the voltage drop is measured over the two inner fingers, we infer a contact resistance of less than 100 Ω. We note that at low temperatures, where quantum mechanics influences the transport, these measurements have to be interpreted with care. For ballistic transport, every electrode would significantly disturb the system by scattering a considerable amount of electrons into the nanowire [24][25]. In order to obtain the correct resistance, the voltage probes should have much smaller contact transparency than the source and drain electrodes. Nevertheless, we believe that our results provide a good estimate, because the gate-dependent measurements described below indicate diffusive rather than ballistic transport for the considered nanowires even at low temperatures. This is in agreement with systematic studies of the mean free path and scattering in InAs nanowires [26]. For further electrical characterization, the conductive doped Si substrate is used as a global back-gate to perform field effect measurements. In Fig. 6a) the source-drain current is plotted as a function of bias voltage for different back-gate voltages between +20V and –20V. The conduction is n-type, *i.e.* a negative gate voltage reduces the density of mobile electrons and it is possible to completely pinch-off the current through the nanowire.

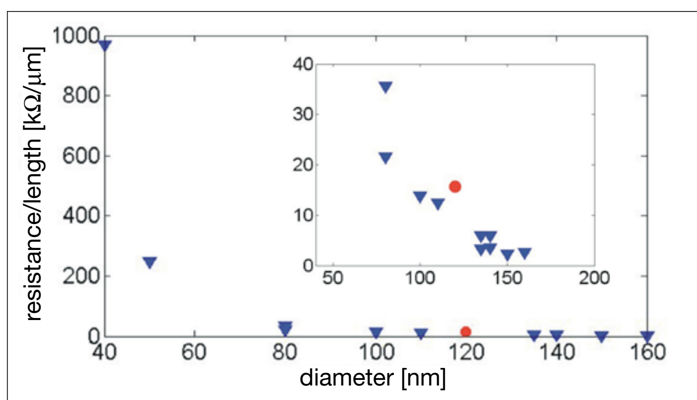

Fig. 5. Diameter dependence of the two terminal resistance per length for nanowires grown in <111> direction (blue triangles) measured at room temperature. Inset: Zoom for d >80 nm. The red circle is the resistance of a representative <001> nanowire.

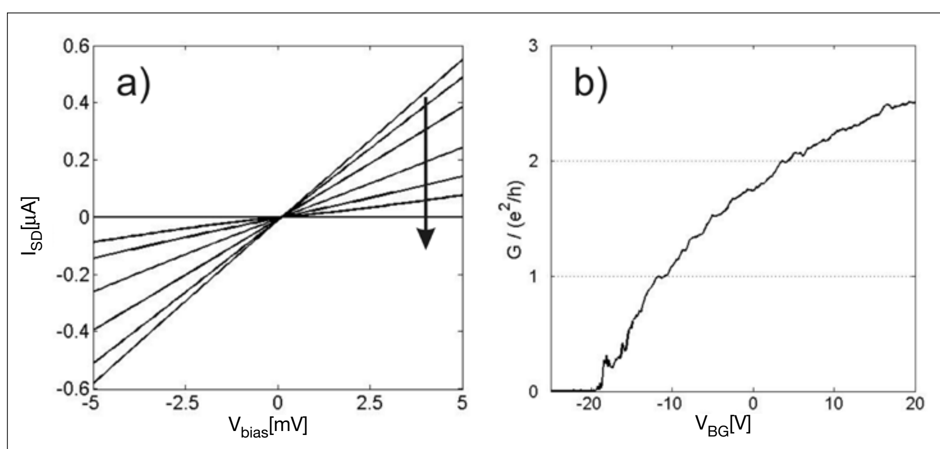

Fig. 6. Electrical measurements on devices as shown in Fig. 4 at T = 4.2 K. a) Source-Drain current as a function of the applied voltage. The voltage on the back-gate is decreased from +20 V to –20 V along the arrow. b) Field effect measurement of the zero bias conductance as a function of back-gate voltage.

Measurement of the differential conductance $G = dI_{SD}/dV_{SD}$ in dependence on the gate voltage is shown in Fig. 6b. It allows the estimation of electron mobility and density with a field-effect transistor (FET) model for a wire-shaped channel on top of a back-gate [27].

For zero back-gate voltage, we find intrinsic carrier densities of $2–5 \times 10^{18}$ cm^{-3}. The origin of this high concentration could be unintentional doping with carbon, which is contained in the metal-organic precursors used in MOVPE. It is however not easy to extract the donor density, since the above-mentioned pinning of the Fermi level in the conduction band at the surface should also lead to a considerable amount of mobile electrons. The carrier mobilities in <111> InAs nanowires are found to be 200–1500 cm^2/Vs. This value is much smaller than theoretical expectations of more than 10^6 cm^2/Vs for one-dimensional electron channels in perfect crystalline heterostructures [28], but it is still about two orders of magnitude larger than for the intensively studied silicon nanowhiskers [29]. In a three-dimensional diffusive system this mobility would correspond to a mean free path of less than 100 nm. A reason for these findings might be scattering at stacking faults along the growth direction for <111> InAs nanowires as described above (Section 2.3). Since this kind of structural changes is not expected for growth in <001> orientation, we compare the resistivity of both types of nanowires. As shown in Fig. 5, no improvement is found for <001> wires. The main scattering mechanism therefore seems to be of a different nature. Because of the electron accumulation at the surface, alternative suggestions attribute the short mean free path to scattering at surface states. This is compatible with the diameter dependence of the resistance shown in Fig. 5, which indicates an abrupt transition to high resistivities for nanowire diameters smaller than 80 nm. Further possible reasons for this may be an increasing contact resistance for smaller diameters or the effect of the narrow lateral confinement pushing the lowest transverse modes above the Fermi level.

Despite the diffusive nature of transport in long nanowires, coherent electronic effects can be experimentally probed in regions confined to sizes shorter than the mean free path. In the following section, our results on quantum dots defined along the nanowire are described.

4. Quantum Dots in Nanowires

In semiconductor quantum dots, only a relatively small number of mobile carriers are confined to a sub-micrometer sized region. Electrons (or holes respectively) occupy discrete quantum levels corresponding to the situation known from basic atomic physics. Quantum dots are therefore often considered as ‘artificial atoms’ with properties that can be tailored at will during fabrication and tuned with gate electrodes as described below.

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If the island is only weakly coupled to electric contacts by tunnel barriers, charges can be added or removed to the dot. An important characteristic is the classical charging energy needed to add another electron from the contact at the cost of the Coulomb repulsion energy. For low enough temperatures, the charging energy is larger than the thermal fluctuations. The quantum dot can then act as a single-electron transistor (SET), if the energy levels inside the island are tuned with a gate electrode. Current through the SET is switched on and off when the energy level corresponding to a certain number N of electrons on the island are in or off resonance with the electrochemical potentials in the source and drain contacts. The off-state of the SET is usually referred to as the Coulomb blockade. Since no carriers can enter or leave the dot in this situation, the number of charges is then completely fixed. On resonance, a finite current can flow and the charge on the island fluctuates between N and N+1 [2].

Under suitable conditions, also the level spacings between the quantum states of the individual electrons become larger than the thermal energy. In this case not only classical Coulomb blockade, but also the quantum mechanical shell structure of the addition spectrum can be probed experimentally [3]. Single charges and individual spins can be controlled in quantum dots in a coherent way, making them promising for the realization for quantum bits (qubits) in solid-state based quantum computation schemes [4].

Quantum dots have already been realized with various methods in semiconductor nanowires.

Early attempts use the whole nanowire itself between weakly transparent contacts to form an island which can be charged and discharged [30][31], similar to devices demonstrated in CNTs. Alternatively, quantum dots were defined along the nanowire by incorporation of barriers made of different material during growth [11]. The resulting dots show highly resolved single-level features and can be emptied up to the very last electron. In both attempts, Coulomb blockade was tuned with a global back-gate and the transparency of the tunnel barriers could not be adjusted independently.

Local gating is an important step for precise control over quantum states and the integration of nanowires into larger nanoelectronic circuits. We therefore focus on improvements of previous attempts to form quantum dots within the nanowire [32] where both the barriers and the energy levels can be tuned with local electrostatic gates. Fig. 7a shows an SEM image of one of the measured devices. Source (S) and drain (D) ohmic contacts to the nanowire are fabricated with optical lithography as described in Section 3.1. In a second step, top-gates are defined with electron beam lithography (EBL). The gate-fingers have a width and separation of about 70 nm. In contrast to the contacts, no etching and surface passivation was done before deposition of 10 nm Cr and 100 nm Au. The native oxide layer on the surface of the nanowire, as shown in Fig 2e, electrically insulates the gates from the wire. Typical breakthrough voltages are above ±1.5 V.

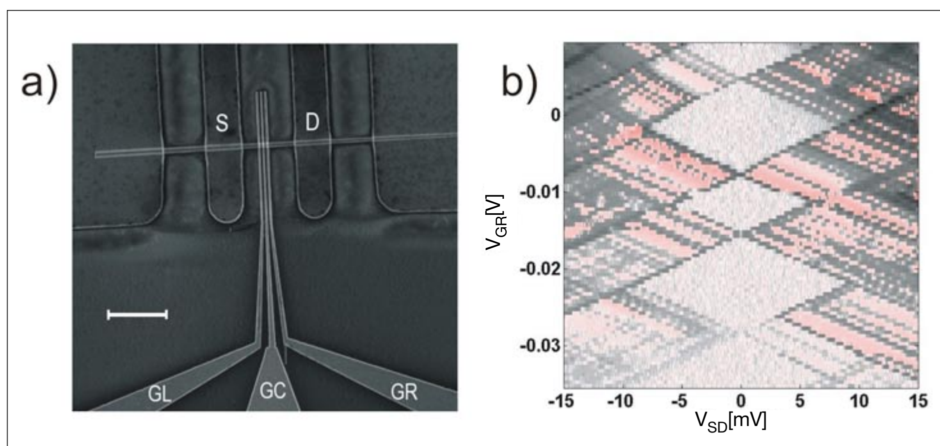

Fig. 7. a) InAs nanowire with ohmic contacts (S, D) and three top-gates (GL, GC, GR). The scale bar is 2 µm. b) Color scale plot $G = dI_{SD}/dV_{SD}$ for a dot formed between GR and GC. The voltage V_{GC} is varied proportional to V_{GR} and for each step, the bias voltage V_{SD} is swept. The measurement was done at low temperature (T = 30 mK).

A single quantum dot is formed by applying a negative voltage to two of the top-gates (GC and GR). This builds up potential barriers for the electrons in the nanowire. The gate GL is kept at a positive voltage during this experiment. A bias voltage is applied between source (S) and drain (D) and the current through the quantum dot is measured at low temperatures in a dilution refrigerator with 30 mK base temperature. In Fig. 7b, the differential conductance $G = dI_{SD}/dV_{SD}$ is plotted with a color scale as a function of the voltage on the top-gate GR and the bias V_{SD}. The voltage V_{GC} is varied proportional to V_{GR} to ensure symmetric barriers. Inside the typical 'diamonds', the current is suppressed due to Coulomb blockade. Other features clearly demonstrate the pronounced influence of quantum mechanics on electronic transport through the dot. The size of the diamonds varies corresponding to the shell filling of this artificial atom. At certain electron numbers, especially stable configurations are formed leading to an increased addition energy. Lines running parallel to the edges of the diamonds are related to transport through excited single particle states in the dot [2][3].

Beyond local gating, we investigated the possibility to create quantum dots by locally changing the shape and hence the potential landscape of the nanowire. One method to create nanometer-sized constrictions is local anodic oxidation with a scanning force microscope (SFM) [33]. Here, a negative voltage is applied to the tip of an SFM, which can be located at a specified position. In controlled temperature and humidity, the semiconductor is locally oxidized in the vicinity of the tip due to an ac-

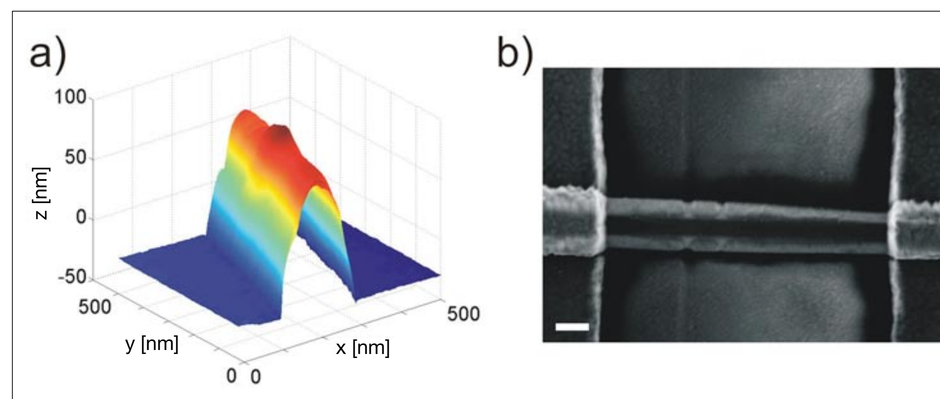

Fig. 8. a) Scanning Force Microscope topography of a piece of InAs nanowire. An oxide spot has been created by local anodic oxidation in humid ambience. b) SEM image of a locally etched nanowire. The trenches have been predefined by EBL and etched in a dilution of HBr and HNO_3. The scale bar is 200 nm.

tivation of the electrochemical reaction by the strong local electric field. Oxidation effectively removes parts of the semiconductor and hence a local constriction is formed. Fig. 8a shows a topographical image of a piece of a nanowire with an oxide spot created by the described method. The image was recorded with the same SFM tip right after the oxidation.

Quantum dots have been realized in InGaAs quantum wells by local etching of geometrical constrictions into lithographically defined channels [34]. In line with that, we used EBL to write 30 nm wide lines into standard EBL-resist (PMMA) over the nanowire. After exposure and development, the sample was etched in a dilution of HBr and HNO_3 (conc.) in water (1:2000). An SEM image of the resulting trenches can be seen in Fig. 8b.

5. Conclusions

InAs nanowires can be grown in a controlled way with MOVPE. Their electrical properties are governed by elastic scattering with a mean free path of around 100 nm. We found evidence that elastic scattering at stacking faults, which frequently occur in <111> grown wires, is not the carrier mobility limiting factor. We realized quantum dots with fully tunable barriers by local top-gates and studied alternative approaches based on geometrical constrictions. At low temperatures, Coulomb blockade measurements reveal a pronounced shell filling spectrum and transport is strongly affected by quantum mechanics.

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